What is claimed is:

1	 A photovoltaic solid state relay having a pair of output
2	terminals, comprising:
3	light emitting means for emitting light in response to an electrical
4	control signal;
5	first and second photovoltaic devices optically coupled to said light
6	emitting means for converting said light to first and second voltages,
7	respectively;
8	first and second unipolar transistors having first and second
9	controlling electrodes for respectively receiving said first and second voltages
10	and jointly establishing a first current conducting path between said output
11	terminals; and
12	a bipolar transistor having a base connected to a junction between said
13	first and second unipolar transistors for establishing a second current
14	conducting path in parallel to said first current conducting path between said
15	output terminals in one of opposite directions depending on voltages applied
16	to said output terminals.

- 2. The photovoltaic solid state relay of claim 1, wherein said first and second unipolar transistors and said bipolar transistor comprise:
- 3 a semiconductor substrate;

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- 4 a first insulator layer on said substrate;
- 5 a semiconductor layer on said first insulator layer;
- 6 first and second backgate regions formed in said semiconductor layer;
- first and second source regions respectively formed in said first and second backgate regions;
- a common drain/base region formed in said semiconductor region
 between said first and second backgate regions;
- 11 a first insulated gate electrode bridging said first source region and

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said common drain/base region, and a second insulated gate electrode 12 bridging said second source region and said common drain/base region; 13 a second insulator layer on said semiconductor layer; 14 first and second gate pads formed on said second insulator layer and 15 respectively connected to said first and second insulated gate electrodes to 16 function as said first and second controlling electrodes of the unipolar 17 transistors; 18 19 a first source pad formed on said second insulator layer and connected to said first source region and said first backgate region and a second source 20 21 pad formed on said second insulator layer and connected to said second 22 source region and said second backgate region, said first and second source 23 pads being respectively connected to said output terminals, said common drain/base region functioning as a common drain of 24 25 said first and second unipolar transistors and as said base of said bipolar 26 transistor, 27 said first and second backgate regions respectively functioning as an emitter and a collector of said bipolar transistor when said first source pad is 28 29 biased at a voltage higher than said second source pad, and respectively 30 functioning as a collector and an emitter of the bipolar transistor when said 31 second source pad is biased at a voltage higher than said first source pad. 1 3. The photovoltaic solid state relay of claim 2, 2 wherein said first backgate region and said first source region are in 3 the shape of a first loop and said second backgate region and said second source region are in the shape of a second loop on the outer side of said first 4 loop, 5 6 wherein said common drain/base region is in the shape of a loop between said first and second loops, and 7 wherein said first insulated gate electrode is in the shape of a loop 8

lying on said first loop and said second insulated gate electrode is in the

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10 shape of a loop lying on said second loop.

- 1 4. The photovoltaic solid state relay of claim 3, wherein said semiconductor layer is formed with first and second wells of conductivity 2 type opposite to conductivity type of said semiconductor layer, said first well 3 being surrounded by said common drain/base region and said common 4 drain/base region being surrounded by said second well, said first and 5 6 second wells penetrating through said semiconductor layer to said first insulator layer. 7
- 5. 1 The photovoltaic solid state relay of claim 2 or 3, wherein said 2 second insulator layer is of a two-layered structure including a field oxide 3 layer immediately above said semiconductor layer.
- 1 6. The photovoltaic solid state relay of claim 2 or 3, wherein said first and second source pads are formed above said first 2 and second wells, respectively, and 3 4 wherein said first and second gate electrodes are formed within said 5 first and second source pads, respectively.
- 7. The photovoltaic solid state relay of claim 1 or 2, wherein said 2 light emitting means comprises a first light emitting diode optically coupled 3 to said first photovoltaic device and a second light emitting diode optically 4 coupled to said second photovoltaic device.
- 8. 1 The photovoltaic solid state relay of claim 1, further comprising: 2 a first discharging circuit connected between said first photovoltaic device and said first unipolar transistor for discharging energy stored in said 3 first unipolar transistor at the instant said first voltage becomes nonexistent, 4 5 and

- a second discharging circuit connected between said second
- 7 photovoltaic device and said second unipolar transistor for discharging
- 8 energy stored in said first unipolar transistor at the instant said second
- 9 voltage becomes nonexistent.